`timescale 1ns / 1ps

////////////////////////////////////////////////////////////////////////////////

// Company:

// Engineer:

//

// Create Date: 00:04:15 06/26/2022

// Design Name: main\_code

// Module Name: D:/morning cep/FPGA\_CEP/test\_bench.v

// Project Name: FPGA\_CEP

// Target Device:

// Tool versions:

// Description:

//

// Verilog Test Fixture created by ISE for module: main\_code

//

// Dependencies:

//

// Revision:

// Revision 0.01 - File Created

// Additional Comments:

//

////////////////////////////////////////////////////////////////////////////////

module test\_bench;

// Inputs

reg Start;

reg Clock;

reg Reset;

reg [1:0] Memory\_Selector;

// Outputs

wire [10:0] Pattern\_Result;

// Instantiate the Unit Under Test (UUT)

main\_code uut (

.Start(Start),

.Clock(Clock),

.Reset(Reset),

.Memory\_Selector(Memory\_Selector),

.Pattern\_Result(Pattern\_Result)

);

always

begin

Clock = 1'b0;

#10;

Clock = 1'b1;

#10;

end

initial

begin

Reset = 1'b1;

#10

Reset = 1'b0;

end

initial begin

// Initialize Input

Start = 1'b1;

Memory\_Selector = 2'b10;

#10;

end

endmodule